REMARKS

Applicants have studied the Office Action dated January 3, 2003 and have made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 1-21 and 30-35 are pending.[1] Claims 1, 7, 8, 15, and 17-19 have been amended, and new claims 30-35 have been added. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks are respectfully requested.

As an initial matter, Applicants note that while a PTO-1449 form (citing the references cited by both the Examiner and Applicants during prosecution of the parent application) was submitted along with the present application, a copy of the PTO-1449 form indicating that all of the cited references were considered by the Examiner was not attached to the present Office Action. Applicants respectfully request that the Examiner consider the references cited in the PTO-1449 form that was submitted with the present application, and attach to the next correspondence a copy of the PTO-1449 form indicating that all of the references cited therein have been considered. For the convenience of the Examiner, enclosed is a copy of the PTO-1449 form that was submitted along with the present application.

Turning to the patentability of the application, the title of the invention was objected to as not being descriptive. The title has been amended to be more clearly indicative of the invention to which the claims are directed.

Claims 1-14 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants have amended claim 1 in light of the specific comments of the

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[1] Applicants note that claims 22-29 were canceled in paragraph 5 of the "Request for Filing a Divisional Application" filed with the present application. Thus, only claims 1-21 were pending before the filing of this Amendment.

Examiner, and submit that all pending claims are now clear and definite. Therefore, it is respectfully submitted that the rejection of claims 1-14 under 35 U.S.C. § 112, second paragraph, should be withdrawn.

Claims 1-10, 12-19, and 21 were rejected under 35 U.S.C. § 102(e) as being anticipated by Iwata et al. (U.S. Patent No. 6,255,702). Claims 11 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata et al. These rejections are respectfully traversed.

The present invention is directed to processes for forming a low resistivity titanium silicide layer at the surface of a silicon semiconductor substrate. One embodiment of the present invention provides a method for forming a low resistivity titanium silicide layer on a surface of a doped region of a silicon semiconductor substrate. According to the method, a titanium layer is deposited on the surface of the doped region of the silicon semiconductor substrate, with the doped region being an n-type or p-type source or drain region. An effective amount of a metallic element is introduced at the interface between the titanium layer and the doped region of the silicon semiconductor substrate so as to promote titanium silicide transformation from C49 phase to C54 phase during a subsequent rapid thermal annealing. The metallic element is chosen from the group consisting of indium, gallium, tin, and lead.

After the introducing step, a rapid thermal annealing of the silicon semiconductor substrate is performed in order to form titanium silicide. Because the effective amount of the metallic element is provided at the interface between the titanium layer and the n-type or p-type doped region of the silicon semiconductor substrate, titanium silicide transformation from the C49 phase to the C54 phase is promoted during the rapid thermal annealing. Thus, a low resistivity titanium silicide layer is formed on the surface of the doped region of a silicon semiconductor substrate.

The Iwata reference discloses a process for forming a semiconductor device in which a silicon nitride film is used in place of a silicon oxide film. However, Iwata does not disclose a method in which a titanium layer is deposited on the surface of an n-type or p-type doped region of a silicon semiconductor substrate, an effective amount of indium, gallium, tin, or lead is

introduced at the interface between the titanium layer and the doped region of the silicon semiconductor substrate so as to promote titanium silicide transformation from C49 phase to C54 phase during a subsequent rapid thermal annealing, and a rapid thermal annealing is performed so as to form titanium silicide, as is recited in amended claim 1. Amended claim 15 contains similar recitations.

Iwata is directed to a semiconductor device fabrication process in which source or drain regions are doped with donors or acceptors through a silicon nitride film rather than a silicon oxide film. See Iwata at 4:9-14. Figures 14(a) through 17(k) of Iwata disclose a process for forming a silicide layer by depositing a silicon nitride film 407 over a silicon semiconductor substrate 401. Iwata at 29:27-30. Indium or boron ions 411 are implanted as acceptors for the silicon substrate 401. Iwata at 29:41-49. Side wall spacers 412 are formed. Iwata at 29:50-51. The silicon nitride film 407 is removed, and then a titanium film 416 is deposited. Iwata at 30:11-13. Next, silicon is ion implanted such that the concentration hits a peak at the interface of the titanium nitride film and the source, drain, and gate electrode regions. Iwata at 30:40-44.

A first rapid thermal anneal is then performed at 675°C to form a C49 phase titanium silicide film. Iwata at 30:47-53. Boron ions 420 are then implanted as acceptors for the silicon substrate, and then the titanium nitride film is removed. Iwata at 31:1-9. A second rapid thermal anneal is then performed at 1000°C to transform the titanium silicide film into the C54 phase. Iwata at 31:9-12. Thus, in the fabrication process of Iwata, a region of the substrate is doped by implanting indium or boron ions as acceptors, then titanium silicide contacts are formed, and then boron ions are implanted as acceptors. Indium is only implanted as an acceptor (i.e., to form a p-type region), and can even be replaced by boron. Iwata does not teach or suggest using introducing indium as a promoter for the silicidation of the titanium layer.

In contrast, in preferred embodiments of the present invention, a supplementary metallic element is added at the interface between a titanium layer and a region that is (separately) doped with any suitable element so as to form an n-type or p-type source or drain region. For example, the metallic element can be deposited on the surface of the doped region or implanted into the doped region. The supplementary metallic element is introduced in an amount that is sufficient to promote titanium silicide transformation from C49 phase to C54 phase during a subsequent

rapid thermal annealing operation. Thus, the metallic element is added as a supplementary element for promoting silicidation.

Iwata does not teach or suggest a semiconductor fabrication method in which an effective amount of indium, gallium, tin, or lead is introduced as a supplementary element at the interface between a region that is separately doped with any suitable element and an overlying titanium layer so as to promote silicidation of the titanium layer. In the process of Iwata, two annealing operations must be performed in order to obtain C54 phase titanium silicide because a supplementary metallic element is not provided as a promoter for silicidation of the titanium layer. The introduction of a supplementary metallic element in preferred embodiments of the present invention provides advantageous results that are not provided by the process disclosed in Iwata. See, e.g., specification at Figure 2.

Applicants believe that the differences between Iwata and the present invention are clear in amended claims 1 and 15, which set forth methods according to preferred embodiments of the present invention. Therefore, claims 1 and 15 distinguish over the Iwata reference, and the rejection of these claims under 35 U.S.C. § 102(e) should be withdrawn.

As discussed above, claims 1 and 15 distinguish over the Iwata reference, and thus, claims 2-14 and claims 16-21 (which depends from claim 1 and 15, respectively) also distinguish over the Iwata reference. Additionally, Applicants submit that limitations in the dependent claims are absent from the Iwata reference. For example, claims 7 and 18 recite depositing the metallic element on the surface of the doped region of the silicon semiconductor substrate. Iwata does not teach or suggest depositing indium, gallium, tin, or lead at the surface of a doped region of a substrate to promote silicidation of a titanium layer. Therefore, it is respectfully submitted that the rejections of claims 1-21 under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a) should be withdrawn.

Claims 30-35 have been added by this amendment, and are provided to further define the invention disclosed in the specification. Claims 30-35 are allowable for at least the reasons set forth above with respect to claims 1-21. Furthermore, Applicants submit that limitations in the

new claims are absent from the Iwata reference. For example, new claims 30, 31, 33 and 34 recite that the doped region of the substrate is an n-type region and/or that it is doped with arsenic. Iwata does not teach or suggest introducing a metallic element such as indium into an n-type source or drain region or a region doped with arsenic. Additionally, such a feature is contrary to the conventional teaching of using such elements as acceptors in p-type regions, and not adding them to an n-type region. However, this feature produces very advantageous, unexpected results. For example, Figure 2 shows the advantageous results obtained when indium was implanted as a silicidation promoter in an arsenic-doped n-type region.

In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

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APPENDIX

IN THE TITLE:

PROCESS FOR FORMING A LOW RESISTIVITY TITANIUM SILICIDE LAYER ON A SILICON SEMICONDUCTOR SUBSTRATE [AND THE RESULTING DEVICE]

IN THE CLAIMS:

1. (Amended) A method for forming a low resistivity titanium silicide layer on a surface of a doped region of a silicon semiconductor substrate, said method comprising the steps of:

depositing a titanium layer on the surface of the doped region of the silicon semiconductor substrate, the doped region being an n-type or p-type source or drain region;

introducing an effective amount of a metallic element at the interface between the titanium layer and the doped region of the silicon semiconductor substrate so as to promote titanium silicide transformation from C49 phase to C54 phase during a subsequent rapid thermal annealing, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead; and

[sometime] after the introducing step, performing a rapid thermal annealing of the [titanium-coated] silicon semiconductor substrate to form titanium silicide.

7. (Amended) The method as defined in claim 1, wherein the introducing step includes the sub-step of depositing the effective amount of the metallic element on the surface of the doped region of the silicon semiconductor substrate.

8. (Amended) The method as defined in claim 1, wherein the introducing step includes the sub-step of implanting the effective amount of the metallic element into the doped region of the silicon semiconductor substrate.

15. (Amended) A method for fabricating a semiconductor device, said method comprising the steps of:

depositing a titanium layer on the surface of at least one n-type or p-type doped region of a silicon semiconductor substrate;

introducing [a predetermined] an effective amount of a metallic element at the interface between the titanium layer and the at least one doped region of the silicon semiconductor substrate so as to promote titanium silicide transformation from C49 phase to C54 phase during a subsequent rapid thermal annealing, the metallic element being chosen from the group consisting of indium, gallium, tin, and lead; and

after the introducing step, performing a rapid thermal annealing of the silicon semiconductor substrate to form a low resistivity titanium silicide layer.

17. (Amended) The method as defined in claim 15, wherein the [predetermined] effective amount of the metallic element is 1×10^{13} to 5×10^{14} atoms/cm^2.

18. (Amended) The method as defined in claim 15, wherein the introducing step includes the sub-step of depositing the [predetermined] effective amount of the metallic element on the surface of the at least one doped region of the silicon semiconductor substrate.

19. (Amended) The method as defined in claim 15, wherein the introducing step includes the sub-step of implanting the [predetermined] effective amount of the metallic element into the at least one doped region of the silicon semiconductor substrate.